REMARKS

I. Status of Application

By the present Amendment, Applicant amends claims 1 and 8. Claims 1 and 3-8 are all the claims pending in the Application, with claims 1 and 8 being in independent form. Claims 1 and 3-8 have been rejected.

The present Amendment addresses each point of objection and rejection raised by the Examiner. Favorable reconsideration is respectfully requested.

II. Formalities

The Examiner has not indicated whether the formal drawings submitted on April 5, 2004 are accepted, as requested by Applicant with the previous Amendment filed on May 9, 2007. Therefore, Applicant again requests that the Examiner approve the aforementioned formal drawings.

III. Claim Rejections Under 35 U.S.C. §102

Claims 1, 3-5, 7 and 8 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by newly cited U.S. Patent No. 7,158,727 to Pathak et al. (hereinafter "Pathak"). Applicant respectfully traverses these rejections for *at least* the reasons set forth below.

According to the MPEP, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (MPEP § 2131). Applicant respectfully submits that claims 1, 3-5, 7 and 8 positively recite limitations which are not disclosed (or suggested) by Pathak.

A. Independent Claim 1

For example, independent claim 1 recites (among other things):

> ...a frequency multiplicator unit, which frequency-multiplies the converted electrical

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data signal, thereby producing a frequency-
multiplied signal; and
     a clock recovery unit comprising a phased
locked loop circuit,
     wherein the frequency-multiplied signal is
used to drive the phase locked loop circuit...
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However, Pathak fails to disclose or even remotely suggest the above features. Indeed, Pathak bears no relevance at all to the invention recited in claim 1 since Pathak does not relate in any way to the question of how a clock signal is recovered from a distorted optical signal. According to the system taught in Pathak, clock recovery must occur at the optical to electrical converter 101, which performs optical to electrical conversion and 1:4 demultiplexing. This is because the optical to electrical converter 101 must have a decision gate that decides, for each bit, whether the bit is 1 or 0. Further, such a decision gate must be clocked at the bit rate of the signal. This process is also referred to as "sampling[1]."

But, Pathak is completely silent regarding the feature of how a clock signal is recovered from a distorted optical signal, because such clock signal recovery is simply not what Pathak's purported invention is concerned with[2]. In stark contrast to Pathak's disclosure, as explained in the present specification, for example, the claimed invention is directed to a novel receiver device for optical data signals which has an improved tolerance for dispersion. As explained in the specification, when transmitting high bit rate optical signals in optical fibers over long distances, such transmitted optical signals is subject to dispersion and such dispersion effects

[1] *See e.g.,* column 1, lines 59-62, "[i]n optical-to-electrical converter 101, the data is typically sampled at the 2.4 GHz rate and a phase adjustment is made on the sampling clock for optimal data recovery."

[2] *See* column 1, lines 62-63, "[t]his requires phase lock loop techniques beyond the scope of this description" (emphasis added).

reduce the optical power within the transmitted optical signal. Hence, it is difficult to recover a clock signal that is needed for the decision process (i.e., for sampling the received signal after optical to electrical conversion so as to recover the original digital bitstream therefrom.

A clock signal may be generated by a phase locked loop that is driven with an analog input signal and a spectral distribution of such a signal is shown in FIG. 1 of the present specification. A filter can be used to select the spectral component at the data rate. Since the spectral component is low due to dispersion effects, the invention recited in claim 1, for example, utilizes an integer fraction or submultiple of this frequency, filters that spectral component (which has significantly higher signal power)[3] and applies frequency multiplication to this signal.

Moreover, as recited in claim 1, a frequency multiplicator unit frequency-multiplies the converted electrical data signal, thereby producing a frequency-multiplied signal, which serves as an auxiliary signal to drive the phased locked loop circuit that of the clock recovery unit. Pathak nowhere discloses, or even remotely suggests this remarkable and unexpected feature. Accordingly, Applicant submits that claim 1 is not anticipated by Pathak for *at least* these reasons.

In addition, Applicant notes that claim 1 explicitly recites the feature of a frequency multiplicator unit, which frequency-multiplies the converted electrical data signal. The Examiner alleges that the electrical-to-optical converter / 4:1 multiplexer 108 performs a frequency multiplication. Applicant respectfully disagrees.

[3] Note that FIG. 1 uses a logarithmic scale.

The feature of frequency multiplication is substantially different from the feature of demultiplexing as disclosed in Pathak. And, MPEP §2111.01 requires that the Examiner give the pending claims their broadest reasonable interpretation. However, Applicant submits that the Examiner's interpretation of a frequency multiplicator unit, which frequency-multiplies the converted electrical data signal, as including a demultiplexer, like that disclosed in Pathak, is not reasonable, as required by the MPEP.

Contrary to the grounds of rejection, the language of claim 1 should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.[4] A skilled artisan would interpret frequency multiplication as being an analog technique used to achieve a spectral transformation. In contrast, a skilled artisan would recognize that demultiplexing is a completely different process of deinterleaving bit streams, which are necessarily digital (not analog).

Therefore, Applicant submits that claim 1 is not anticipated by Pathak for *at least* these additional reasons. Moreover, Applicant submits that claims 3-5 and 7 are allowable over Pathak *at least* by virtue of their dependency. Thus, Applicant respectfully requests that the Examiner withdraw these rejections.

B. Independent Claim 8

In view of the similarity between the requirements of claim 8 and the requirements discussed above with respect to independent claim 1, Applicant respectfully submits that arguments analogous to the foregoing arguments as to the patentability of independent claim 1 demonstrate the patentability of claim 8. As such, it is respectfully submitted that claim 8 is

[4] In re Bond, 910 F.2d 831, 833, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990), citing In re Snead, 710 F.2d 1544, 1548, 218 U.S.P.Q. 385, 388 (Fed. Cir. 1983).

patentably distinguishable over the cited Pathak reference *at least* for reasons analogous to those presented above. Thus, the allowance of this claim is respectfully solicited of the Examiner.

IV. Claim Rejections Under 35 U.S.C. §103

Claims 1 and 3-8 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Green (6,909,309) in view of Pathak et al. (7,158,727). As already explained in detail above, Pathak fails to disclose or suggest all the recitations of claims 1 and 3-8. Further, Green fails to remedy the deficient teachings of Pathak. Therefore, claims 1 and 3-8 are patentable over Pathak, Green, and any combination thereof, *at least* for reasons analogous to those presented above and the allowance of these claims is respectfully solicited of the Examiner.

V. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

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